Design Checklist for LTC388X Family of PSM Buck Converters

by Michael Jones

INTRODUCTION

Please follow this checklist to insure a working LTC388X board design. If you make any exceptions to these checks, please call your local LTC Field Application Engineer for advice.

POWER CIRCUIT

1. ☐$INTV_{CC}$
    a. ☐10.0uF min bulk cap (10V X7R) to PGND
    b. ☐0.1uF ceramic to PGND
    c. ☐If V_{IN} is below 6V, tie $INTV_{CC}$ to V_{IN} and add 1-2.2Ohm resistor between bulk C and 4.7uF at pin
    d. ☐Do not drive externally
2. ☐Output Filter
    a. ☐Proper sized L that will not saturate or overheat
    b. ☐Proper sized C that will give correct peak to peak voltage
    c. ☐Reasonable DCR/ESR losses
3. ☐Input Filter
    a. ☐Use bulk and ceramic capacitor (X5R/X7R), locate ceramic next to MOSFET
    b. ☐Make sure input filter will not cause resonance with converter
4. ☐Current sensing and voltage sensing.
    a. ☐DCR kelvin sensing lines, and R/C properly connected
    b. ☐DCR V_{DCR} scaled properly
    c. ☐DCR resistor divider if signal too large
    d. ☐DCR Bias currents compensated with R
    e. ☐DCR Bias current R has 1uF in parallel
    f. ☐Resistor sensing lines properly connected (kelvin sense) and power dissipation checked
    g. ☐Resistor sensing pi filter

5. ☐Temperature Sensing (Output Inductor)
    a. ☐Make Sure the PNP sensing transistor is close to inductor
6. ☐Power MOSFET Switches
    a. ☐Top switch optimized for switching losses (low Qgd)
    b. ☐Bottom switch optimized resistive losses (low Rdson)
    c. ☐Ensure gate threshold is logic level
7. ☐Gate drive
    a. ☐ Add 1-5Ohm boost pin resistor in series with the boost pin to reduce switch ringing. Connect one end of the resistor to the pin, and connect the other end to the diode and capacitor,
8. ☐Compensation
    a. ☐R/C pole/zero in place
    b. ☐Filter C on ITH pin and SGND

DIGITAL/LOGIC

1. ☐Connect Logic/coordination signals
    a. ☐Tie all ALERTB together
    b. ☐Tie all SCL/SDA together, pull up to 3.3V with one 10K Resistor
    c. ☐Tie all SHARE_CLK together, pull up to 3.3V with one 10K
    d. ☐Tie all Run0/Run1
    e. ☐Tie all WP together, pull down to Ground with one 0 Ohm Resistor
2. ☐Addressing
    a. ☐ASELs (double check correct values)
    b. ☐ Check for collision with other devices on the bus and any global addresses published in their datasheets (i.e. cannot use LTC4306)
    c. ☐Must have a single base address for in system programming
        i. It is recommended that you use 0xXF (i.e. 0x4F) as the single, common base address
        ii. You will need to program MFR_ADDRESS (command 0xE6) to this value (i.e. 0x4F)
        iii. Hardware ASELs on 3880 will set the lower nibble directly (0x40 to 0x4F in this example)
3. ☐Open Drain Pins
    a. ☐GPIOn, SYNC, SHARE_CLOCK have 10K pull up to 3.3V
    b. ☐SDA, SCL, SYNC, ALERT/ have 8.33K pull up to 3.3V

c. ☐Adjust pull up if stray C

d. ☐RUN pin should only be driven by open collector to prevent contention and high currents

e. ☐GPIOn should only be driven by open collector to prevent accidental contention and high currents

4. ☐RCONFIG PINS

a. ☐Resistor dividers to V2.5 and SGND

b. ☐1% resistors

c. ☐Values match table entries

d. ☐ASEL values unique

5. ☐Use time base sequencing so faults can be properly shared.

6. ☐Programming

a. ☐Add switch (what kind?) to disconnect dongle 3.3V when VIN present

b. ☐Ensure VIN, V3.3, V2.5 have a high impedance when dongle connected without VIN

c. ☐Do not use any body diodes between SDA/SCL from any slave device

7. ☐Test Points

a. ☐Input

b. ☐Output

8. ☐Polyphase rails

a. ☐Tie all SNYC together

b. ☐ For any given SYNC group, only **one chip** (we call this the frequency master) can specify a FREQUENCY_SWITCH value (i.e. 500kHz). All other chips must specify FREQUENCY_SWITCH=0x8000 ('External Clock')

c. ☐ Check RCONFIG for FREQ_CFG to make sure there is only one master and the phasing is set properly

d. ☐Connect the ITH pins of each phase together

9. ☐ All faults acted upon (fault response is not 'ignore', especially in polyphase applications) must be propagated via MFR_GPIO_PROPAGATE

10. ☐The MFR_GPIO RESPONSE must be inhibit

11. ☐In MFR_PWM_CONFIG_LTC3880 SHARE_CLOCK_ENABLE set to a 1 (default setting)

12. ☐In MFR_CHAN_CONFIG_LTC3880 ShareClkControl set to a 1 (default setting)

REVISION HISTORY

Rev	Date	Description	Page Number