

Design Checklist: LTC297X

Nov 7th, 2014

Design Checklist for LTC297X Family of PSM Mamagers

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INTRODUCTION

Please follow this checklist to insure a working LTC2978/LTC2974 board design. If you make any exceptions to these rules, please call applications to make sure your design will work properly.

POWER CIRCUIT

- 1. Addressing
- 2. The address select pins (ASELs) are tri-level, check the addressing table on Page 22 of the LTC2978 datasheet (LTC2974 has the same addressing scheme).
- 3. Theck for collision with other devices on the bus and any global addresses published in their datasheets (i.e. cannot use LTC4306).
- 4. Must have a single base address for in system programming.
- 5. Connect the output enable pins of LTC297X to the RUN pins of the switchers (call apps engineer immediately if you want otherwise)
 - a. Insure appropriate pullups on all V_{OUT_EN}
 - b. The ABS_MAX voltages of the $V_{OUT_{EN}}$ pins are:
 - i. ☑out_EN[3:0]: -0.3V to 15V (for both LTC2974 and LTC2978)
 - ii. □V_{OUT_EN}[7:4]: -0.3V to 6V (LTC2978)
- 2. Anti-aliasing filters
 - a. Add anti-aliasing filters to the LTC297X inputs VSENSEP, VSENSEM, ISENSEP and ISENSEM.
 - b. The recommended filtering for voltage inputs is 100 Ω and 100nF.
 - c. The recommended filtering for current sensing is $1k\Omega$ and 10nF.
 - d. Add a first stage matched filter when using DCR current sensing.
 - e. There is no need to add an external resistive divider to sense 12V, the VIN_SNS has a calibrated divider built-in.
- 3. Remote Temperature Sensing (LTC2974 only)
 - a. Use a diode-connected PNP or NPN.
 - b. Do*not* use real diodes such as 1N4148 for temperature sensing!
 - c. The ground connection should go back to the LTC2974 local ground.
 - d. Dise up to 330nF decoupling capacitance if the layout is noisy.
 - e. Route the temperature sensing traces away from switch nodes or other noise sources.
- 4. Decoupling Capacitors
 - a. Dise 100nF decoupling capacitors for VPWR, VDD33, VDD25 and between REFP and REFM
- 5. Connect Logic/Coordination signals

- a. All open drain pins (ALERTB, SCL, SDA, SHARE_CLK, FAULTB) should have a single common pull up.
- b. \Box hort all ALERTB together, pull up to 3.3V with a 10k Ω resistor.
- c. Short all SCL/SDA together, pull up to 3.3V with a $10k\Omega$ resistor.
- d. Adjust SDA/SCL pull up or add an I²C bus buffer if stray capacitance is an issue. Check the rising edges of SCL/SDA with an oscilloscope to confirm.
- e. \Box Short all SHARE_CLK together, pull up to 3.3V with a 5.49k Ω resistor
- f. Short all WP together and pull up to 3.3V with a $10k\Omega$ resistor
- g. Do not leave CONTROL pins floating! Pull up to 3.3V with a $10k\Omega$ resistor.
- 6. FAULT Handling
 - a. For maximum flexibility and software control, short all FAULTB pins together and pull up to 3.3V with a single $10k\Omega$ resistor.
 - b. Do not mix power good, fault and control pins to design custom fault-handling or event-based sequencing schemes. These approaches are extremely difficult to debug and do not allow last minute software fixes.
- 7. Floating Inputs
 - a. Connect all unused VSENSEP, VSENSEM and DACM pins to GND.
- 8. Programming
 - a. Use the schematic below for each LTC297X if programming with dongle power only is desired.
 - b. Ensure that VDD33 consumes less than 100mA to avoid overloading the I²C dongle.
 - c. No body diodes between SDA/SCL from any slave device are allowed.



- 9. Trim DAC Resistors
 - a. Select the trim DAC resistors using the resistor-selection tool in the LTpowerPlay GUI
 - b. □From the main menu "Utilities" -> "Resistor Selection Tool"
 - c. Enter the required information in the form (feedback voltage, desired trim range etc.)

D Resistor Selection Tool					
Design Inputs	Driving the Feedback Node of DC/DC's With External Dividers				
Basic Switcher Parameters	EAFETY FEATURE				
Feedback Node Voltage: 0.600 ψ Feedback Resistor R20: 60.400 kl D 0					
Nominal Feedback Node Input Current: 0.0 💼 nA	Low range + 1.54 max High range + 2.74 max				
Optional Switcher Parameters for Worst Case Analysis					
Feedback Node Voltage Tolerance 0.0 👘 % Design Solution					
	Design Summary				
Maximum Feedback Node Input Current: 50.0 🚔 nA	[]				
Tolerance of R20	Value of R10: 90.900 k D U Ω				
Output Voltage and Margining Requirements Value of R30: 237.000 k D U Ω					
✓ Symmetric Margin/Trim	Trim DAC Range: lo range (1.38V fullscale)				
Maximum Output Voltage: 15.0	Design Verification				
Nominal Output Voltage: 1.000 + V Minimum Output Votage: 15.0 +	Param Value Comment Nominal Output Voltage Error: -0.132 % Margin High Range: 15.159 %				
	Margin Low Range: -20.010 %				
Tolerance of Feedback and Trim Resistors	Trim DAC Resolution : 0.034 %/LSB				
Tolerance of B10: 1%	Min Margin Low Range Needed: -0.593%				
Tolerance of R30: 1%	with margin right cargo recording 500 %				
ОК	Cancel				

10. Use the LTpowerPlay GUI to get Factory Apps support. The email alias automatically copies multiple people depending on availability/vacation etc.



REVISION HISTORY

Rev	Date	Description	Page Number